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ChuanKang Liang, Student Member, IEEE, And Behzad Razavi, Fellow, IEEE Abstract—This Paper Proposes A Simulation-based Modeling Methodology That Provides Greater flexibility In The Design And Apr 28th, 2024.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 12 ...Payam Heydari, Senior Member, IEEE Abstract—Integration Of Multi-mode Multi-band Transceivers On A Single Chip Will Enable Low-cost Millimeter-wave Systems For Next-generation Automotive Radar Sensors. The first Dual-band Millimeter-wave Transceiver Operating In The 22–29-GHz And 77–81 Apr 15th, 2024 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 8 ...IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 8, AUGUST 2014 1739 A 7.1 MW 1 GS/s ADC With 48 DB SNDR At Nyquist Rate Sedigheh Hashemi And Behzad Razavi, Fellow, IEEE Abstract—A Two-stage Pipelined ADC Employs A Double-sampling Mar 9th, 2024 2398 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. ...Higher SNDR. The Modulator Achieves 82-dB Dynamic Range And 81-dB Peak SNDR In The A-weighted Audio Signal Bandwidth With An OSR Of 64. The Total Power Consumption Of The Modulator Is 1 MW From A 0.6-V Supply. The Prototype Occupies 2.9 Mm<sup>2</sup> Using A 0.35-μm CMOS Technology. Index Terms—Del Mar 19th, 2024.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11 ...B. Quadrature Clock Generator The PLL Provides Two 1-GHz 50% Duty-cycle Clocks,  $\text{clk}$  And  $\text{clk}_q$  In Fig. 1, That Are Phase Shifted With Respect To One Another By 90°. As Noted In The Introduction, Quadrature Clocks Simplify The Generation Of The Local 2-GHz Clocks That Are Required In Sections Of The SOC That Are Double-pumped In Order Feb 14th, 2024 1944 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. ...A Compact Switched-Capacitor Regulated Charge Pump Power Supply B. Robert Gregoire, Member, IEEE Abstract—A CMOS Switched-capacitor Reference Is Combined With A Switched-capacitor Voltage Doubling Charge Pump To Produce A Compact Regulated 3.2-V Power Supply From An Input That Ranges From 1.8 To 3.5 V. It Can Supply Up To 6 mA At Minimum Input. Mar 13th, 2024 1186 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. ...1188 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 6, JUNE 2010 Fig. 4. Comparison Between (a) A Conventional Current-Switch FFE And (b) A Charge-Injection FFE When Data Pattern Is '011'. Fig. 5. Simulated (a) Current, (b) Voltage, And (c) Current In Fig. 1 When An Isolat Mar 28th, 2024.

1216 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. ...1216 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 6, JUNE 2007 An SC Voltage Doubler With Pseudo-Continuous Output Regulation Using A Three-Stage Switchable Opamp Hoi Lee, Member, IEEE, And Philip K. T. Mok, Senior Member, IEEE Abstract—This Paper Presents A Switched-capacitor Voltage Mar 5th, 2024 1618 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 53, NO. ...Yi Et Al.: BLE RX FRONT END WITH 1.33-nW SLEEP POWER FOR ENERGY-HARVESTING APPLICATIONS IN 28-nm CMOS 1619 Alternatively, The Sub-0.5-V Energy-harvesting Sources Favor The Use Of An Ultra-low-voltage (ULV) Supply To Build An ULP Radio. In [7], The Supply Voltage (VDD) Is Minimized To 0. May 11th, 2024 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 7, ...IEEE JOURNAL OF SOLID-STATE

CIRCUITS, VOL. 34, NO. 7, JULY 1999 949 Low-Power Bandgap References Featuring DTMOST's Anne-Johan Annema Abstract— This Pa Apr 1th, 2024.

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JOURNAL OF SOLID-STATE CIRCUITS, VOL. 50, NO. 2 ...Constraint Is Given By (2) Where, As In (1), Denotes The Time, After The Clock Edge, That And Need To Create A Reasonable Swing At .1 An Interesting Observation In The Above Architecture Is That And (and And ) Can Be Merged Because They Evaluateconcurrently.2 Inotherwords,theflipflo Apr 3th, 2024IEEE

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