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Design And Analysis Of A Low-Power 8-Bit 500 KS/S SAR ADC ...Architecture, Used In This Project, Is Explained In Detail. The Design And Analysis Of Each Sub-system For The ADC System Has Been Explained Thoroughly. Novel Comparator Architecture Is Proposed. This Bulk Input Comparator Substantially Reduces The Overall Power Consumption Of The ADC System. All The Circuits In This Project Were Designed In Apr 5th, 2024

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