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8086 16-BIT HMOS MICROPROCESSOR 8086 8086-2 8086-1 Will Release The Local Bus During T4 Of The Cycle When All The Following Conditions Are Met: 1. Request Occurs On Or Before T2. 2. Current Cycle Is Not The Low Byte Of A Word (on An Odd Address). 3. Current Cycle Is Not The First Acknowledge Of An Interrupt Acknowledge Sequence. 4. A Locked Instruction Is Not Currently Executing. Feb 8th, 2024 8086/8088 Hardware Specifications - WordPress.com • Write Line Indicates 8086/8088 Is Outputting Data To A Memory Or I/O Device. -during The Time WR Is A Logic 0, The Data Bus Contains Valid Data For Memory Or I/O -high-impedance

During A Hold Acknowledge INTA •The Interrupt Acknowledge Signal Is A Response To The INTR Input Pin. -normally Used To Gate The Interrupt Vector Number Mar 12th, 2024

Microcomputer Systems The 8086 8088 Family Architecture

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