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LECTURE 03 - DEEP SUBMICRON (DSM) CMOS TECHNOLOGY Major Fabrication Steps For A DSM CMOS Process 1.) P And N Wells 2.) Shallow Trench Isolation 3.) Threshold Shift And Anti-punch Through Implants 4.) Thin Oxide And Gate Polysilicon 5.) Lightly Doped Drains And Sources 6.) Sidewall Spacer 7.) Heavily Doped Drains And Sources Apr 3th, 2024

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Chapter 4 Low-Power VLSI Design Power VLSI Design Overview Of Power Consumption • The Average Power Consumption Can Be Expressed As $1 \text{ Avg C Load } V_{DD} \text{ C Load } V_{DD} F_{CLK} T P 2$ • The Node Transition Rate Can Be Slower Than The Clock Rate. To Better Represent This Behav May 1th, 2024

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