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EECE488 Analog CMOS Integrated Circuit DesignEECE488 Analog CMOS Integrated Circuit Design Assignment 4 Due: Tuesday November 26th, 2013 At 8:00am 1. Consider The Following Circuit. (This Circuit Is Sometimes Referred To As A Self-biased Current Source). R V_{DD} GND M_0 M_2 M_1 M_3 GND I_{out} Assume All Transistors Are Operating In Saturation Region And $\beta_n = \beta_p = \beta$, $V_{DD} = 3V$, $V_{TH}(NMOS) = 0$... May 9th, 2024Analog And Digital Circuit Design In 65 Nm CMOS: End Of ...Circuit Design Will Be Addressed Such As The Increased Leakage And Variability With Scaling Technologies. Next, The Impact Of This On Digital Circuit Design And

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References: “Analog Integrated Circuit Design” By D. Johns And K. Martin And
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