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Can Easily Modify The Reference Design To Accommodate A Different Analog Interface X-Ref Target - Figure 1 Figure 1: Virtex-6 FPGA DSP Ki Jan 18th, 2024

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Tan-3 Starter Kit -- A User's Guide By Sin Ming Loo, Version 1.02, Boise State University, 2005 ... Design Can Be Set To XST VHDL Or XST Verilog As Shown In Figure 2.3. The Targeted FPGA Device Is A Xilinx Spartan 3 XC3S200 Family Device, Specifically A XC3S200FT256 FPGA (it Is Mar 18th, 2024

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Custom Daughter Board (for The DUT) Was Designed By The NASA Electronic Parts And Packaging (NEPP) Group.The Decision Was Made To Use Custo M Versus A DUT Evaluation Board So That 32-bit Parallel SelectMap -confi Feb 19th, 2024

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Number Of DNA_PORTS: 0 Out Of 1 0% Number Of DSP48E1s: 3 Out Of 840 1% ...

This System Runs Off A Reference Clock Frequency Of 200 MHz From The Differential Clock Source On The Board. The AXI MM ... Push_Buttons_5Bits Axi_gpio 0x40500000 0x4050FFFF Jan 6th, 2024

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Resnet50 [7.7G] 91.65% 91.23% -0.42% 40% 90.79% -0.86% 32% Inception_v2 [4.0G] 91.07% 90.37% -0.70% 60% 90.07% -1.00% 55% SqueezeNet [778M] 83.19% 82.46% -0.73% 89% 81.57% -1.62% 75% Detection Networks Baseline MAP Pruning Result 1 Pruning Result 2 MAP ... Feb 14th, 2024

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