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UTrenchMOS(tm) Standard Level FET
Pder 03aa25 0 40

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PcDE E1 HE L Qwv OUTLINE REFERENCES VERSION
EUROPEAN PROJECTION ISSUE DATE 97-02-28
99-09-13 IEC JEDEC EIAJ Mm 0.1 0.48 0.38 0.15 0.09
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Si9410DY N-channel TrenchMOS™ Logic Level
FETPder (%) 03aa19 0 40 80 120 0 50 100 150 200 (C)
C) Ider (%) Pder Ptot P ... Package Outline Fig 14.
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