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Ping A Circuit Into LUTs As Illustrated In Figure 2. Figure 2a Illustrates Theinitialgate-levelnetwork, Figure2billustrates A Possible Covering Of The Initial Network Using 4-LUTs, And Figure 2c Illustrates The LUT Network Produced By The Cov-ering. In The Mapping Given, The Gate Labele May 12th, 2024

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Prototype The Nuclei Evaluation SoC (included RISC-V Core) In FPGA Boards; And The Nuclei Made JTAG Debugger Kit (called Hummingbird Debugger Kit), Which Can Be Used To Debug The RISC-V Core In FPGA Prototype Or In Real Chip. Figure 1-1 May 8th, 2024

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