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3.3 Setting The Channel Code (WT-101A Only) The WT-101A Transmitter Is Equipped With A 4-position DIP-switch Marked CHANNEL (Fig. 6) That Serves As A Channel Selector. By Means Of This Switch, The Transmitter Can Be Programmed To Activate One Of 4 Outputs At The Receiver. Figure 6. Channel SelectorFile Size: 241KBPage Count: 2 May 3th, 2024

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Chapter 8 Memory Hierarchy And Cache Memory

• Suppose Processor Has 2 Levels Of Hierarchy: Cache And Main Memory • T Cache = 1 Cycle, T MM = 100 Cycles • What Is The AMAT Of The Program From Example 1? AMAT = T Cache + MR Cache (t MM) = [1 + 0.375(100)] Cycles = 38.5 Cycles Memory Performance Example 2 Apr 1th, 2024

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Memory Array Programming Of The Memory Can Be
Delayed To One Of Last Process Steps ROM Layout
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