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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [Mar 2th, 2024

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C0-00dr-d 120 0 C0-00ar-d C0-01dd1-d 140 60
C0-01dd2-d C0-01dr-d 140 0 C0-01ar-d C0-02dd1-d
140 60 C0-02dd2-d 140 0 C0-02dr-d C0-10dd1e-d 120
... C0-11dre-d C0-11are-d 8 Ac Rs-485 + _ Lg
C0-11dd1e-d C1 X1 X2 X3 X4 C2 X5 X6 X7 X8 C3 Y1 Y2
Y3 Y4 C4 Y5 Y6 +v Lnk/act Port1 Pwr Run Err Run Stop
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